AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-11. (Canceled)

12. (Currently Amended) A circuit according to claim ~~11~~ 16, wherein, during the ~~deciphering~~ decryption of the data by the security module, the cache memory ~~breaks~~ divides the deciphered data available at the output of the security module, which has a length greater than the standard data length, into standard-length data.

13. (Currently Amended) A circuit according to claim ~~12~~ 15, wherein the security module uses a secret key algorithm which processes data having a length of at least 64 bits, and wherein the standard length of the data processed by the microprocessor is less than 64 bits.

14. (Previously Presented) A circuit according to claim 13, wherein said secret key algorithm is the AES algorithm.

15. (New) An integrated circuit, comprising:

a microprocessor;

a set of peripheral devices connected to said microprocessor by a bus having a data length that is equal to the standard length of data processed by said microprocessor;

a security module connected to said bus for encrypting and decrypting data;

a communication interface for accessing devices external to the integrated circuit, said communication interface being connected to said security module by a dedicated link that is distinct from said bus, such that data exchanged between said microprocessor and said communication interface is encrypted and decrypted by said security module;

a cache memory that stores data to be provided to the security module for encryption and transfer to an external device via said communication interface; and

a cache memory controller that writes data to the cache memory in units each having a length greater than the standard data length of the data processed by the microprocessor, for encryption by the security module.

16. (New) The integrated circuit of claim 15, wherein said security module decrypts data received from an external device via said communication interface in units that are equal to said length greater than the standard data length, and provides the decrypted data to the cache memory controller for writing to said cache memory in units of said length.

AMENDMENTS TO THE DRAWINGS:

Replace the single sheet of drawings with the accompanying Replacement Sheet.

In the Replacement Sheet, the sole figure has been revised to include labels to identify the structures represented by the blocks, and the cache memory and cache memory controller have been illustrated, as requested by the examiner.